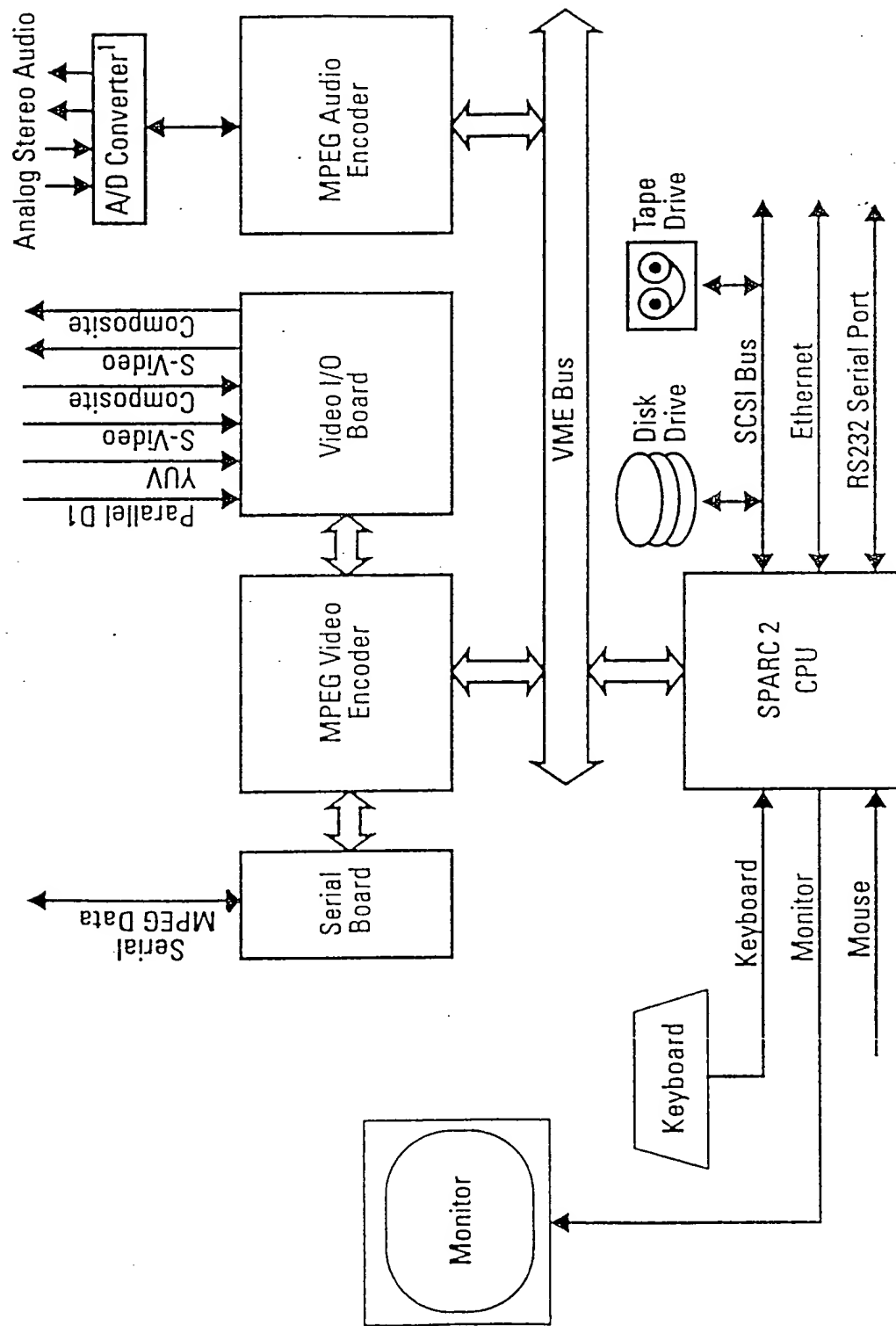


Fig. 1



PRIOR ART

Figure 2

MPEG 2 Encoder Development System, Block Diagram

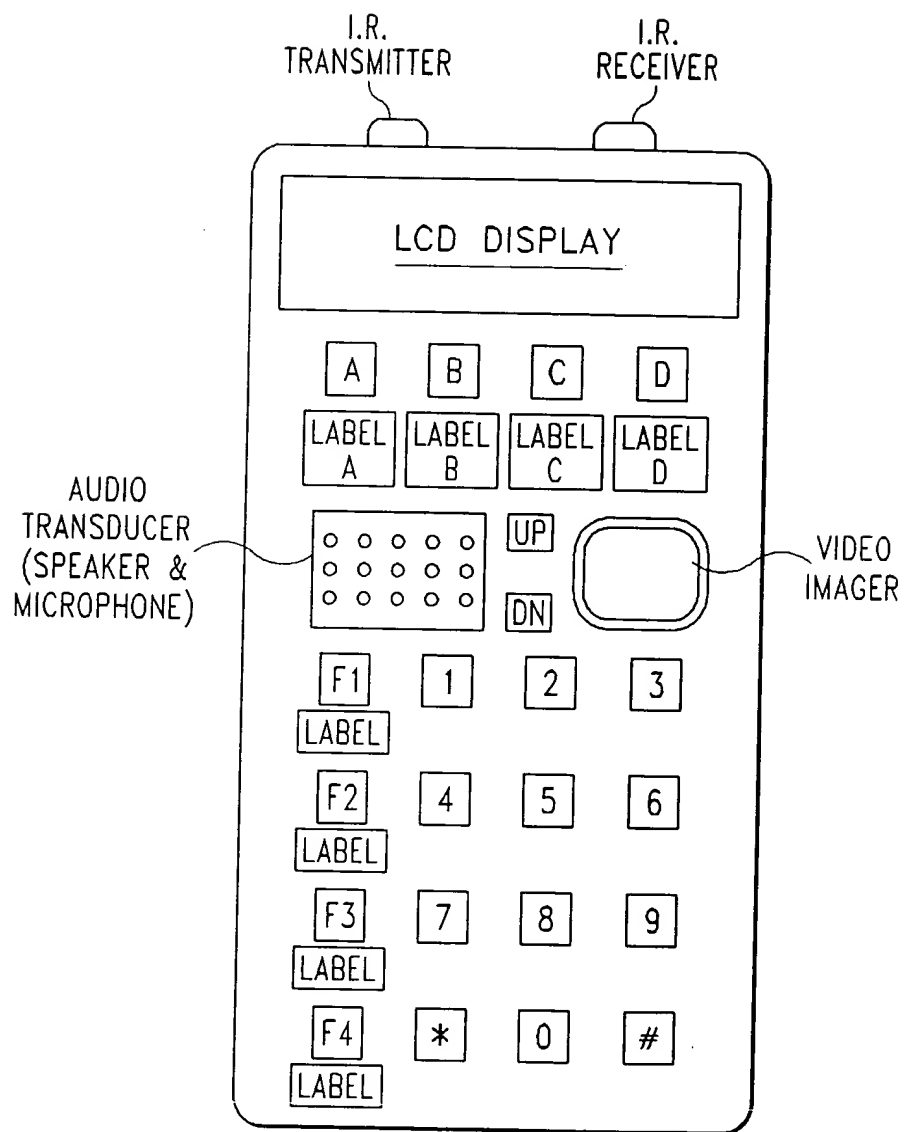


Fig. 3

PROGRAM DATA STREAM NUMBER	IDENTIFIER	PROGRAM STORAGE TIME 1	STORAGE TIME 1 PRIORITY	STORE PERIOD	MOST/ LEAST RECENT OVERWRITE	PROGRAM STORAGE TIME 2	STORAGE TIME 2 PRIORITY	STORE PERIOD	MOST/ LEAST RECENT OVERWRITE
1									
2									
3									
4									
A B C D E F G H I J K L M N O P Q R S T U V W X Y Z 0 1 2 3 4 5 6 7 8 9 * # - : M T W T h F S a S u A M P M									
HOUR DAY WEEK MONTH M-F DAILY WEEKLY S-S MOST LEAST									
<div>EXIT</div>									

Fig. 4

PROGRAM DATA STREAM NUMBER	IDENTIFIER	PROGRAM STORAGE TIME 1	STORAGE TIME 1 PRIORITY	STORE PERIOD	MOST/ LEAST RECENT OVERWRITE	PROGRAM STORAGE TIME 2	STORAGE TIME 2 PRIORITY	STORE PERIOD	MOST/ LEAST RECENT OVERWRITE
1	SPORTS	6:00 PM 7:00 PM M-F	1	1 WEEK	LEAST	2:00 PM END Sa	2	1 WEEK	
2	HOBBIES								
3	NEWS	6:00 PM 6:30 PM M-F	2	2 DAY	LEAST	ALL	3		LEAST
4	MUSIC								

A B C D E F G H I J K L M N O P Q R S T U V W X Y Z
0 1 2 3 4 5 6 7 8 9 * # - : M T W Th F Sa Su AM PM
HOUR DAY WEEK MONTH M-F
DAILY WEEKLY S-S MOST LEAST
EXIT

Fig. 5

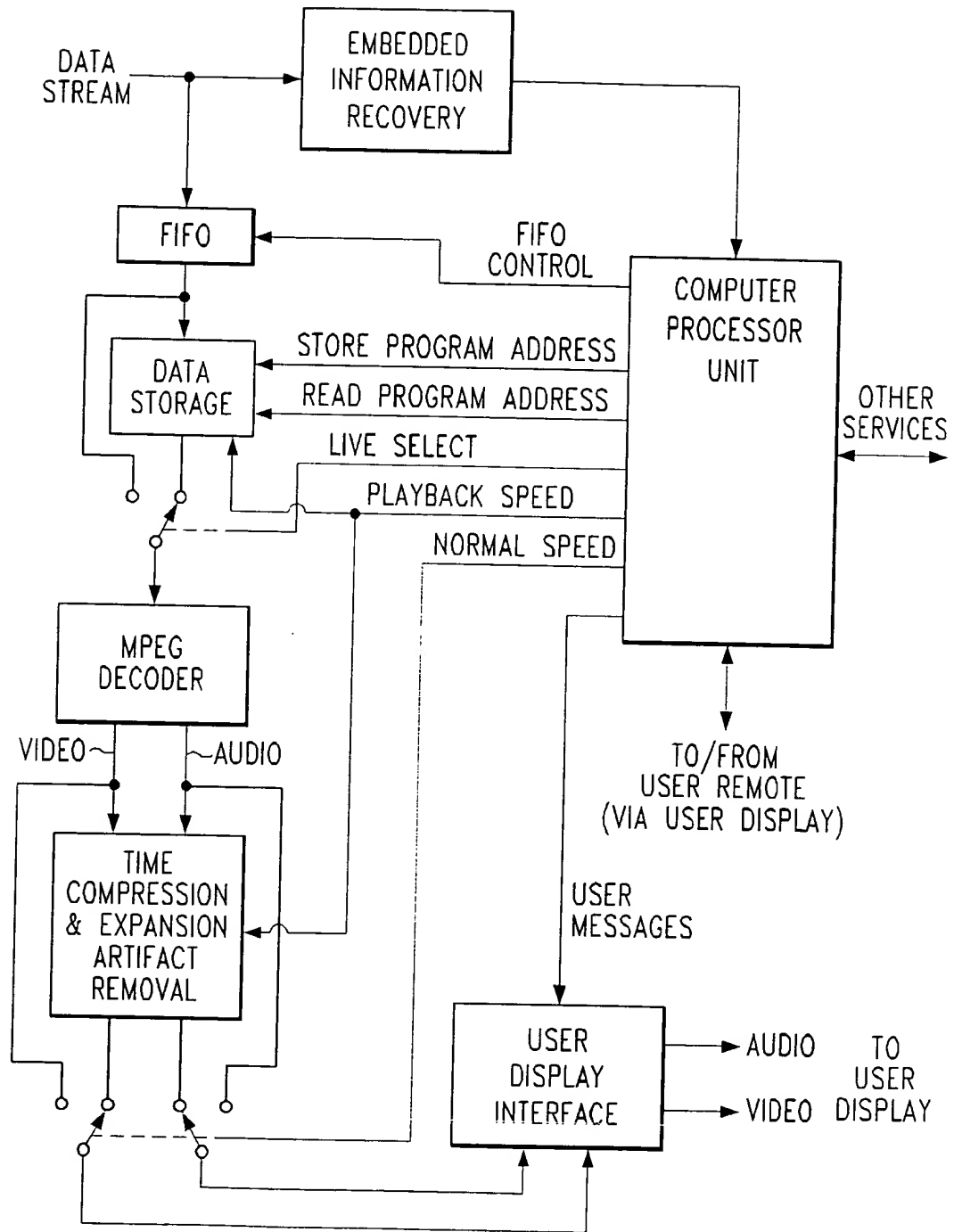


Fig. 6

FIG. 7

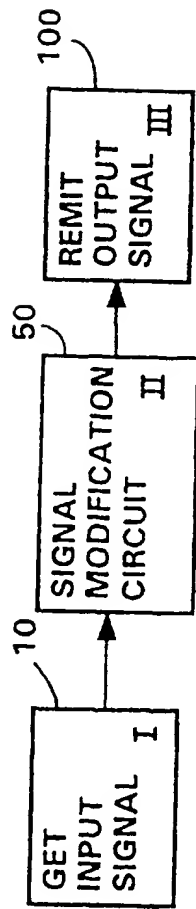


FIG. 8

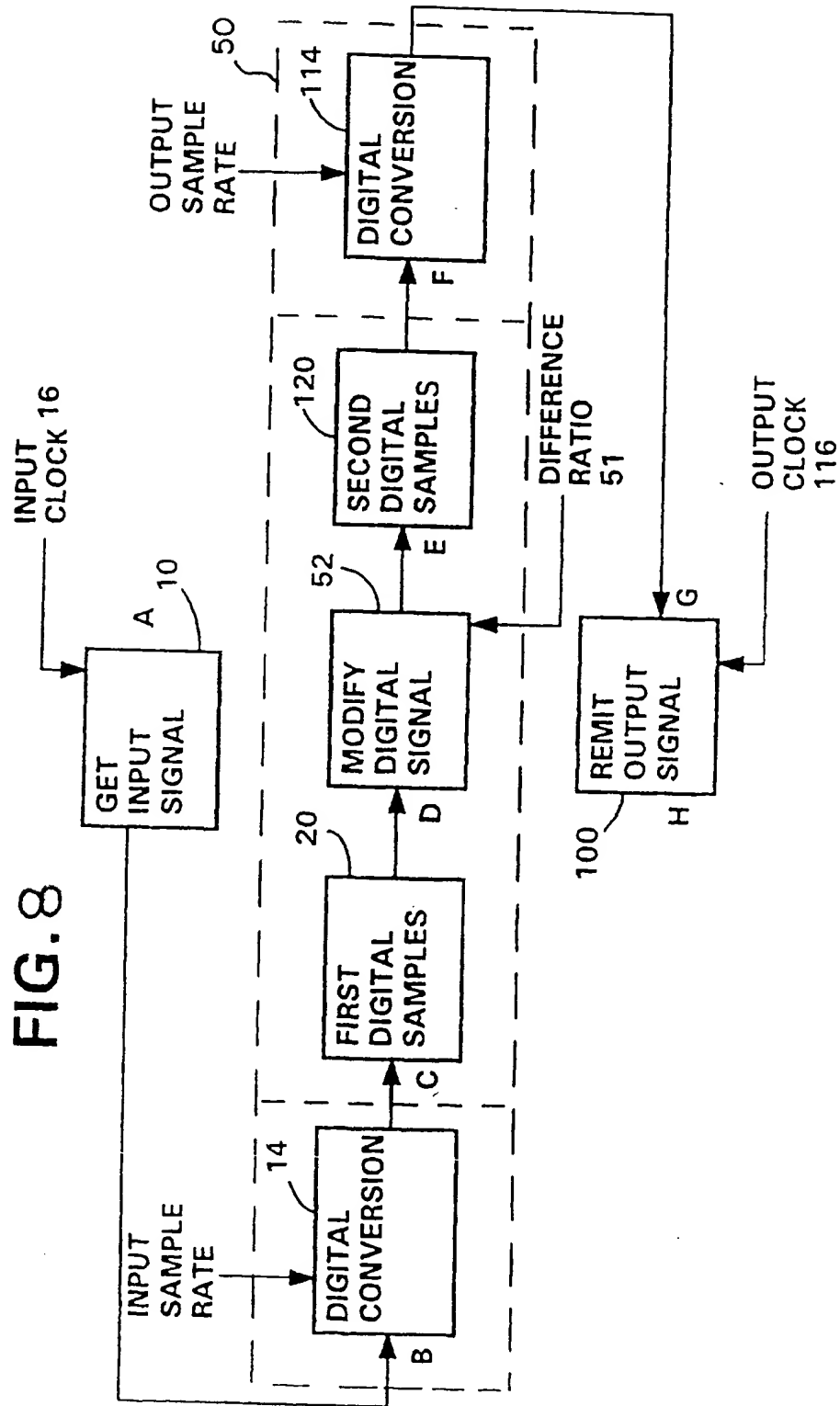


FIG. 9

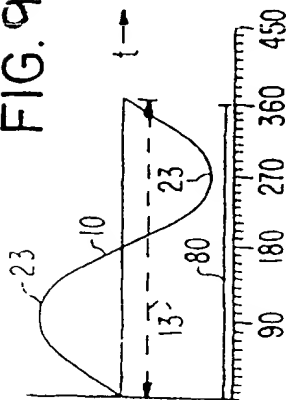


FIG. 10

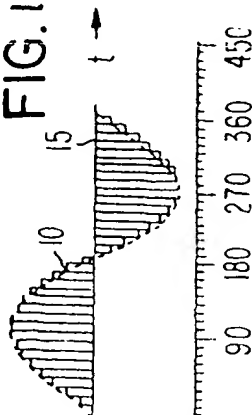


FIG. 11

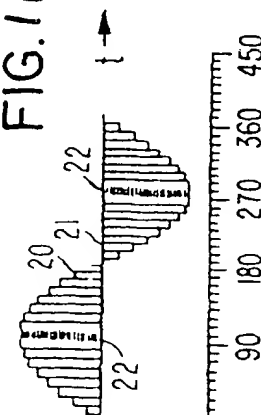


FIG. 12

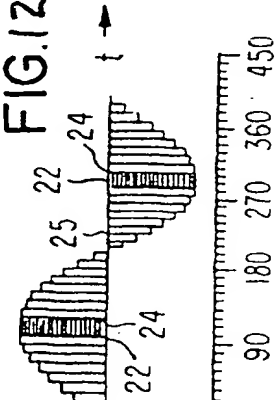


FIG. 13

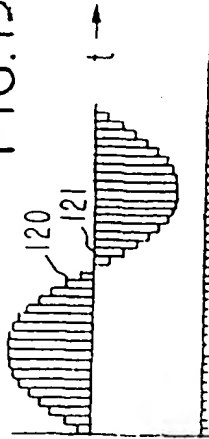


FIG. 14

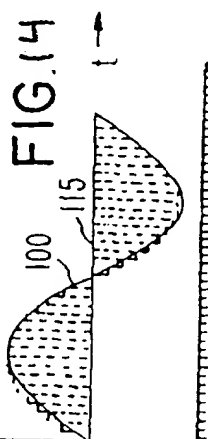


FIG. 15

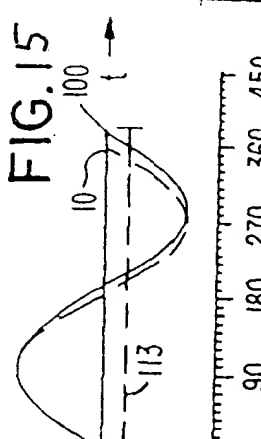


FIG. 16

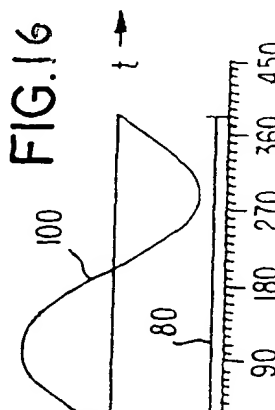


FIG. 17

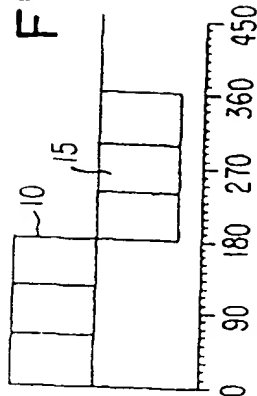


FIG. 18

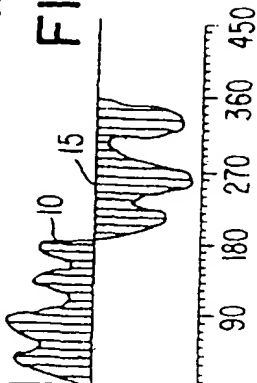


FIG. 19

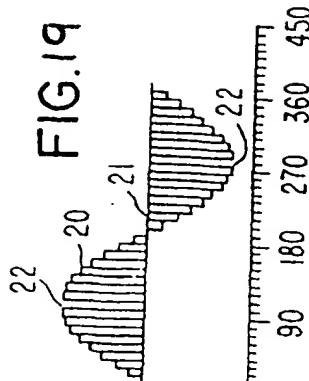


FIG. 20

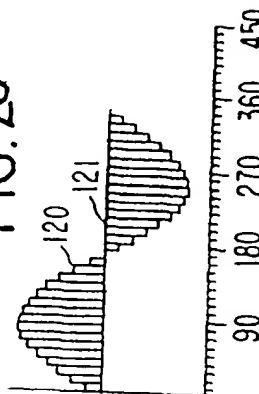


FIG. 21

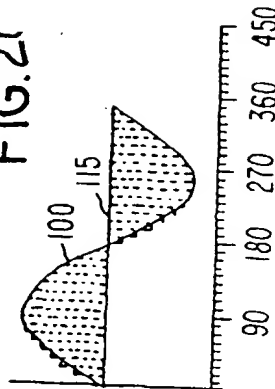


FIG. 22

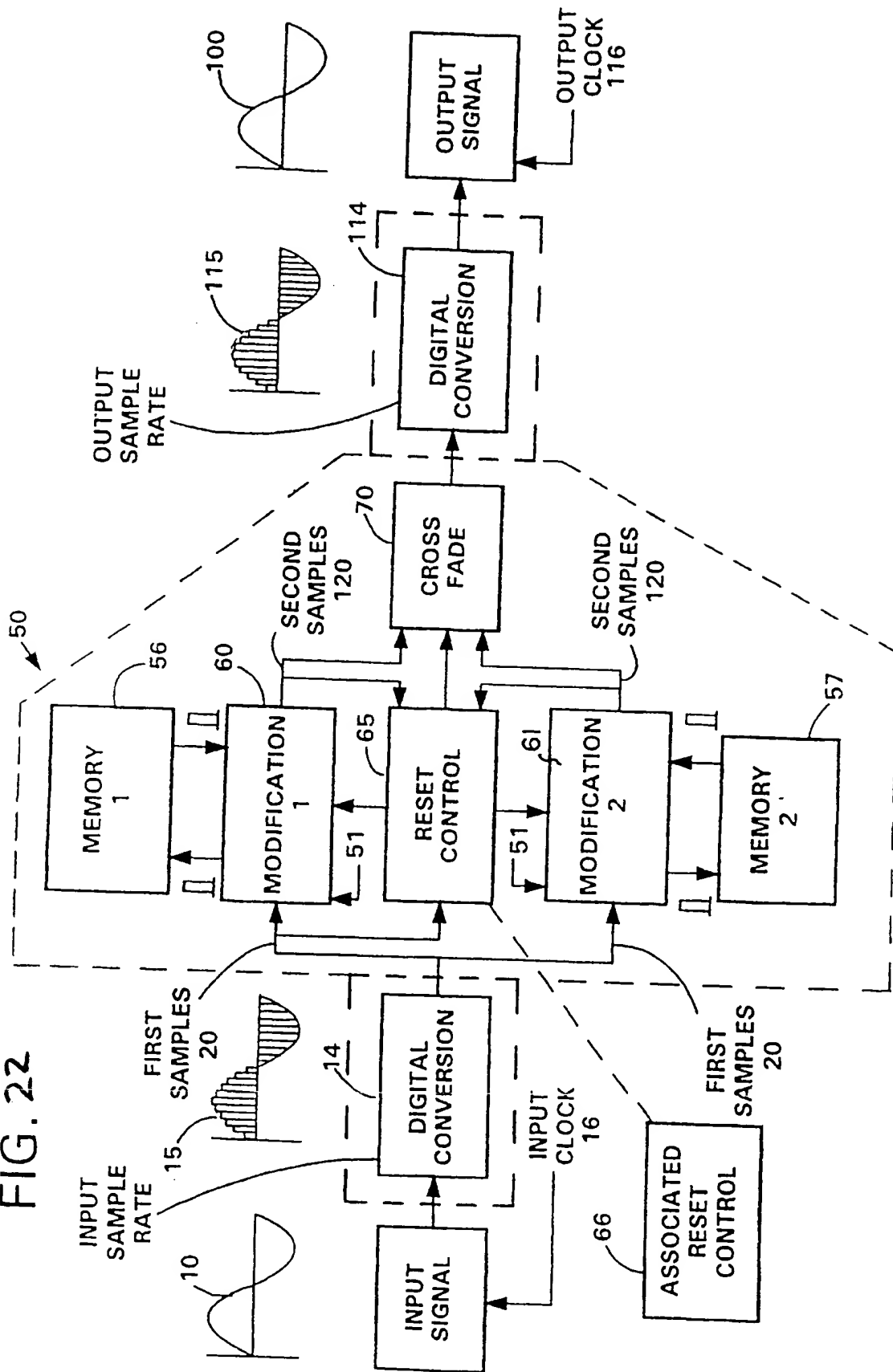


FIG. 23

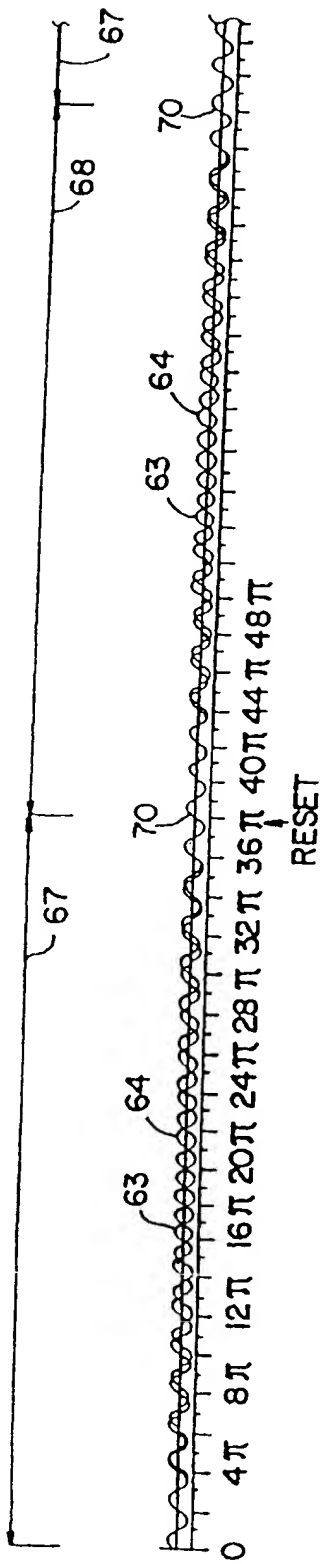


FIG. 24

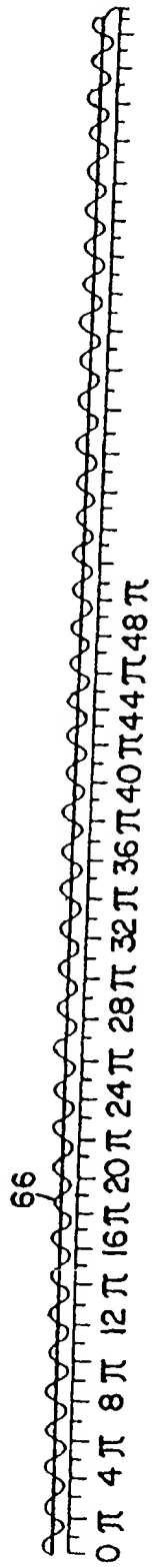


FIG. 25

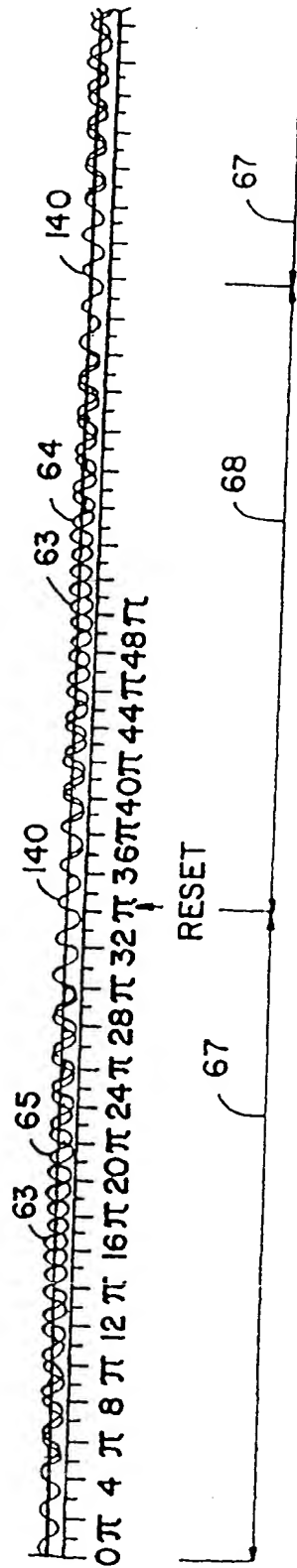


FIG. 26A

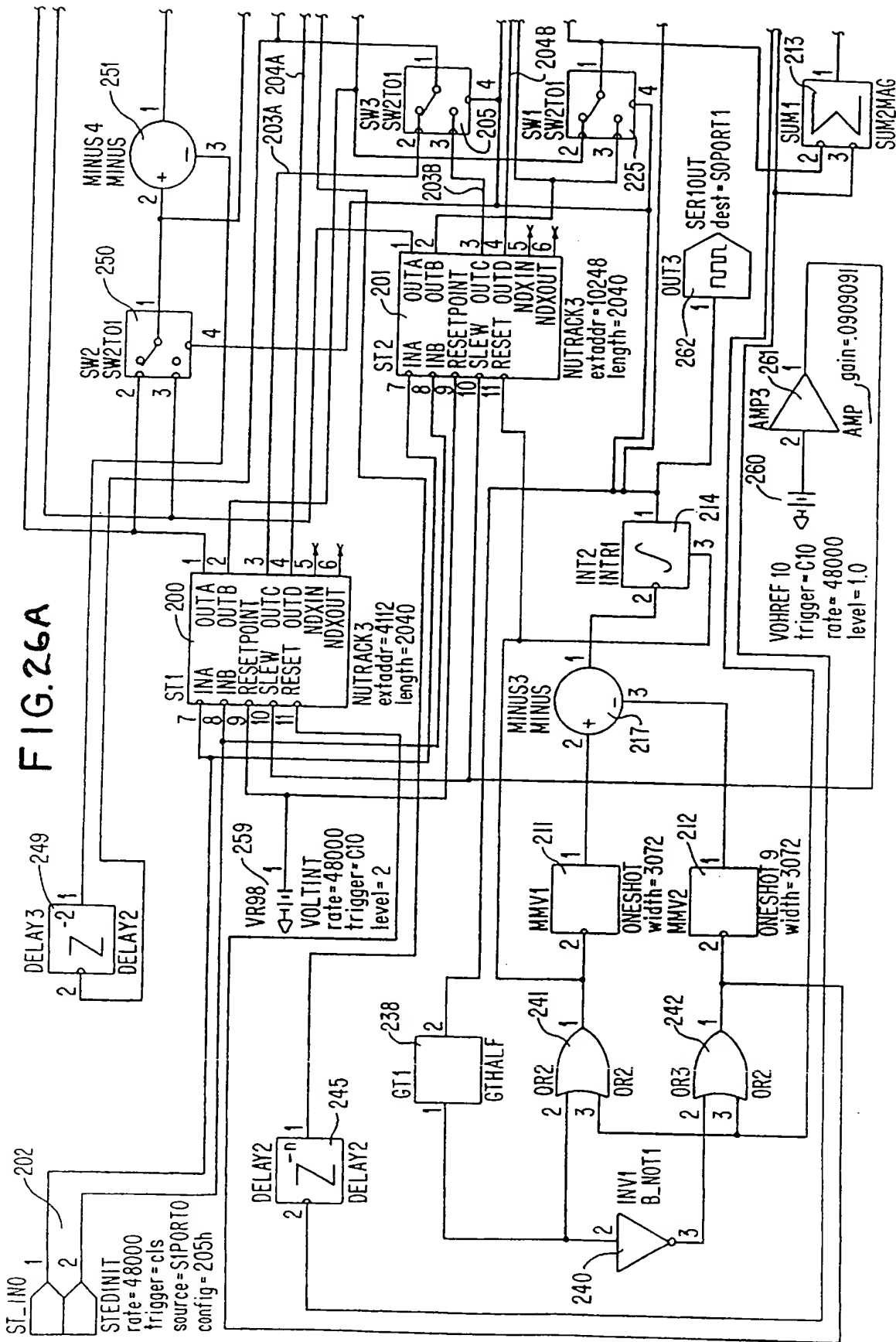


FIG. 26B

FIG. 26B is a detailed block diagram of a signal processing circuit. The circuit includes several input channels (P9, P10, P11) and various processing blocks. Key components include: DIFF4, DIFF5, DIFF6, DIFF7, DIFF8, DIFF9, DIFF10, DIFF11, DIFF12, DIFF13, DIFF14, DIFF15, DIFF16, DIFF17, DIFF18, DIFF19, DIFF20, DIFF21, DIFF22, DIFF23, DIFF24, DIFF25, DIFF26, DIFF27, DIFF28, DIFF29, DIFF30, DIFF31, DIFF32, DIFF33, DIFF34, DIFF35, DIFF36, DIFF37, DIFF38, DIFF39, DIFF40, DIFF41, DIFF42, DIFF43, DIFF44, DIFF45, DIFF46, DIFF47, DIFF48, DIFF49, DIFF50, DIFF51, DIFF52, DIFF53, DIFF54, DIFF55, DIFF56, DIFF57, DIFF58, DIFF59, DIFF60, DIFF61, DIFF62, DIFF63, DIFF64, DIFF65, DIFF66, DIFF67, DIFF68, DIFF69, DIFF70, DIFF71, DIFF72, DIFF73, DIFF74, DIFF75, DIFF76, DIFF77, DIFF78, DIFF79, DIFF80, DIFF81, DIFF82, DIFF83, DIFF84, DIFF85, DIFF86, DIFF87, DIFF88, DIFF89, DIFF90, DIFF91, DIFF92, DIFF93, DIFF94, DIFF95, DIFF96, DIFF97, DIFF98, DIFF99, DIFF100. The circuit also includes several logic gates (AND, OR, NOT), comparators (P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15, P16, P17, P18, P19, P20, P21, P22, P23, P24, P25, P26, P27, P28, P29, P30, P31, P32, P33, P34, P35, P36, P37, P38, P39, P40, P41, P42, P43, P44, P45, P46, P47, P48, P49, P50, P51, P52, P53, P54, P55, P56, P57, P58, P59, P60, P61, P62, P63, P64, P65, P66, P67, P68, P69, P70, P71, P72, P73, P74, P75, P76, P77, P78, P79, P80, P81, P82, P83, P84, P85, P86, P87, P88, P89, P90, P91, P92, P93, P94, P95, P96, P97, P98, P99, P100), and various other functional blocks (SUM4, SUM5, SUM6, SUM7, SUM8, SUM9, SUM10, SUM11, SUM12, SUM13, SUM14, SUM15, SUM16, SUM17, SUM18, SUM19, SUM20, SUM21, SUM22, SUM23, SUM24, SUM25, SUM26, SUM27, SUM28, SUM29, SUM30, SUM31, SUM32, SUM33, SUM34, SUM35, SUM36, SUM37, SUM38, SUM39, SUM40, SUM41, SUM42, SUM43, SUM44, SUM45, SUM46, SUM47, SUM48, SUM49, SUM50, SUM51, SUM52, SUM53, SUM54, SUM55, SUM56, SUM57, SUM58, SUM59, SUM60, SUM61, SUM62, SUM63, SUM64, SUM65, SUM66, SUM67, SUM68, SUM69, SUM70, SUM71, SUM72, SUM73, SUM74, SUM75, SUM76, SUM77, SUM78, SUM79, SUM80, SUM81, SUM82, SUM83, SUM84, SUM85, SUM86, SUM87, SUM88, SUM89, SUM90, SUM91, SUM92, SUM93, SUM94, SUM95, SUM96, SUM97, SUM98, SUM99, SUM100). The circuit is designed to process multiple input signals and generate a final output signal based on a complex set of logic and arithmetic operations.

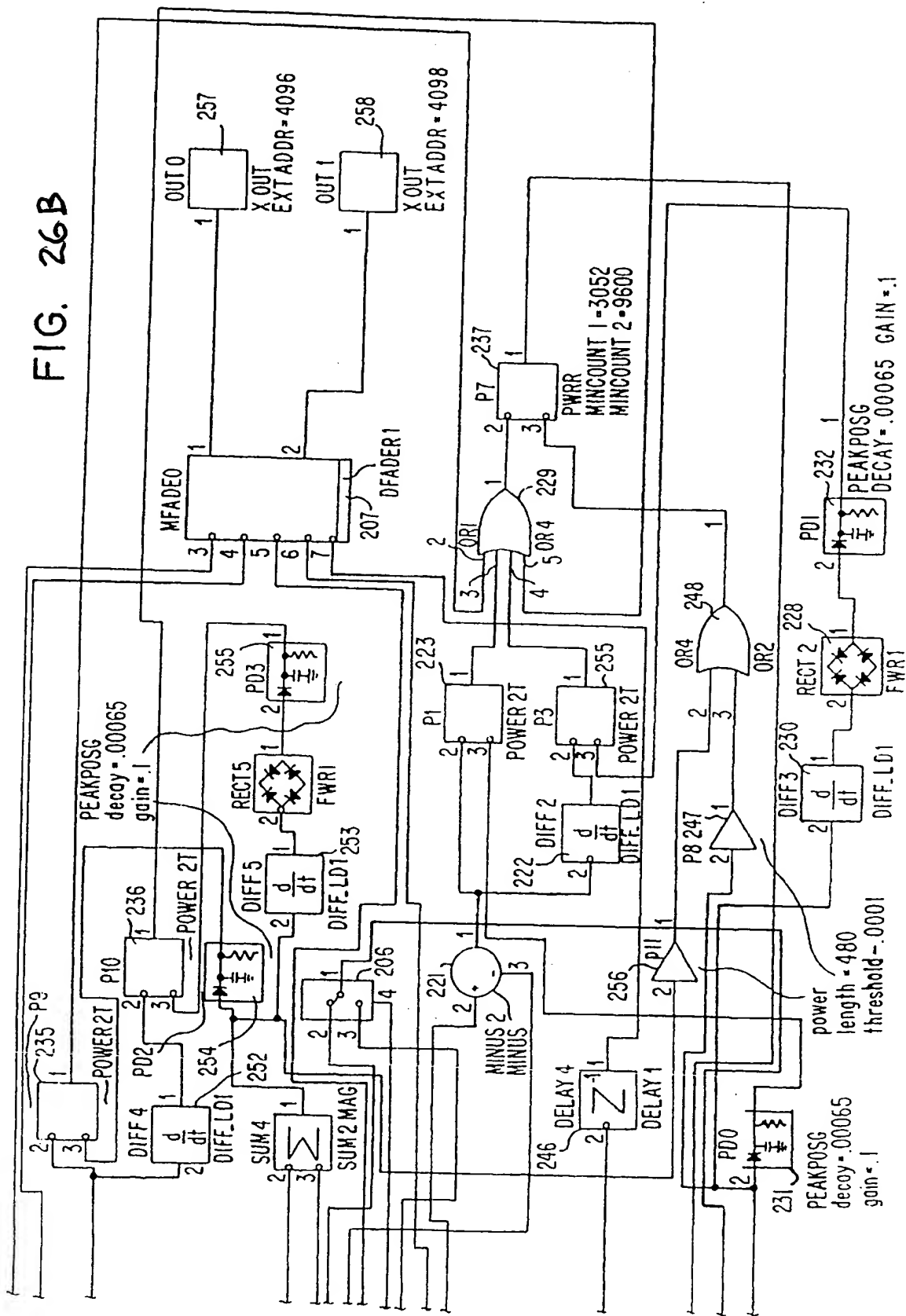


FIG. 27A

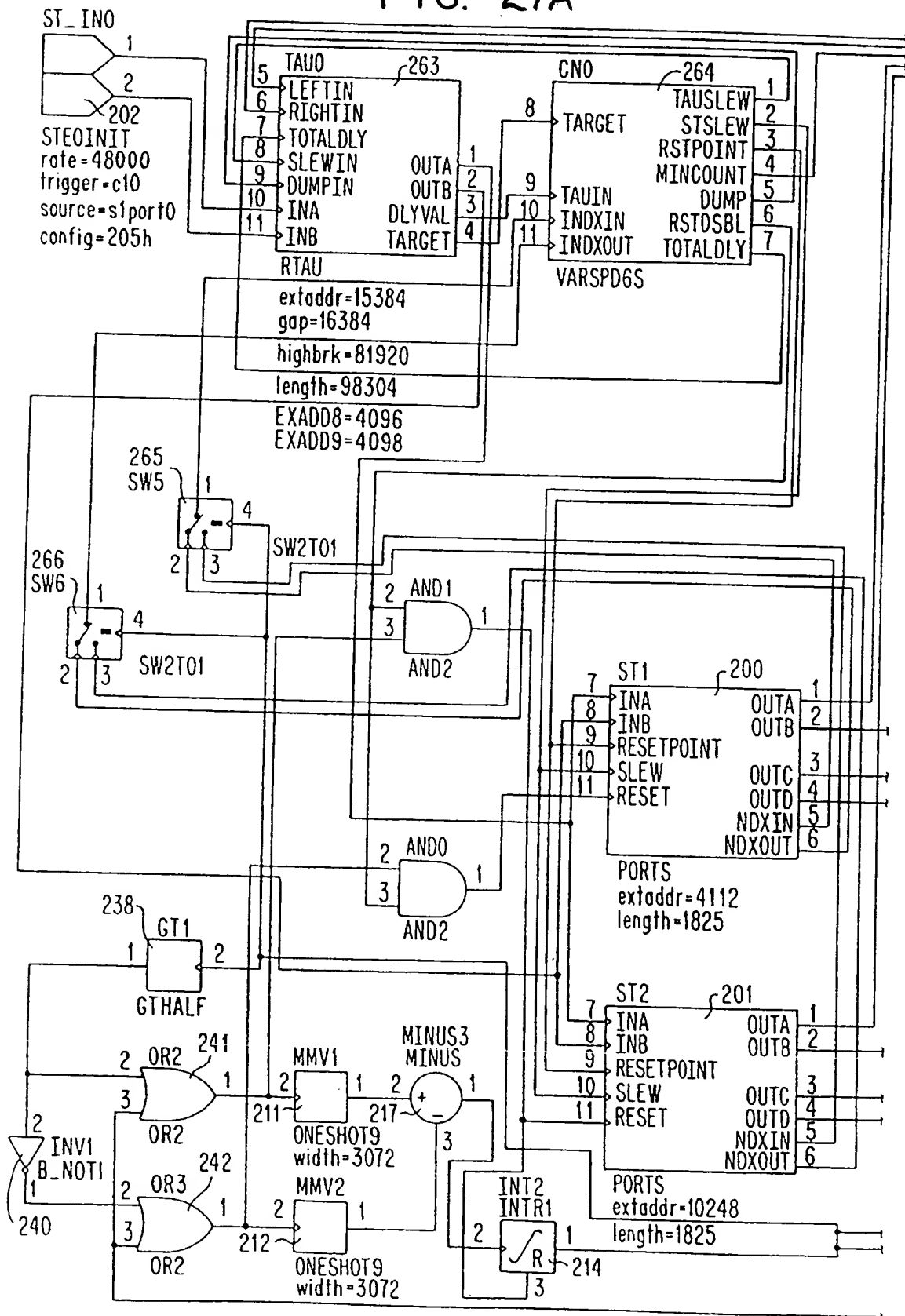


FIG. 27B

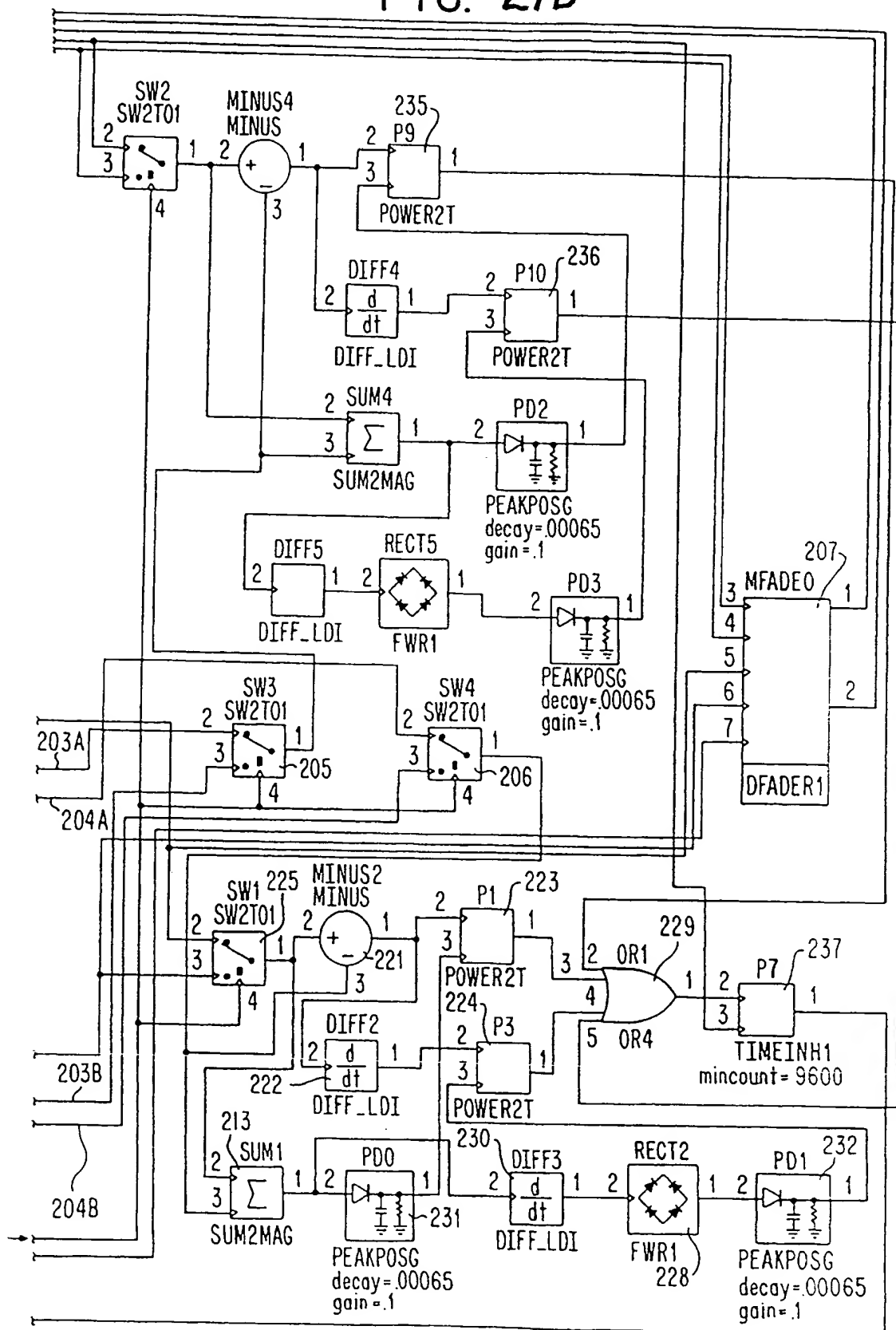


FIG. 28

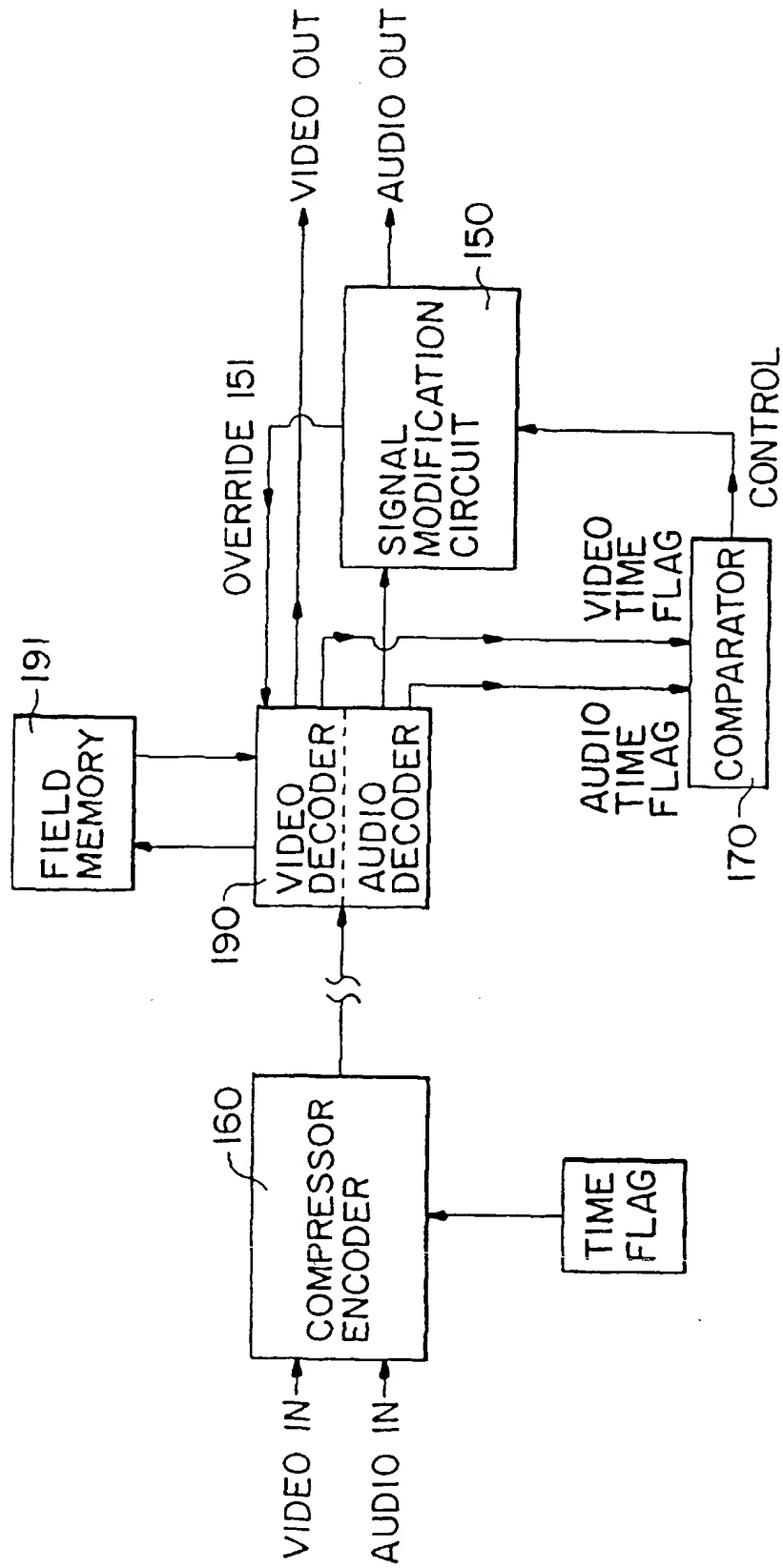


FIG. 29

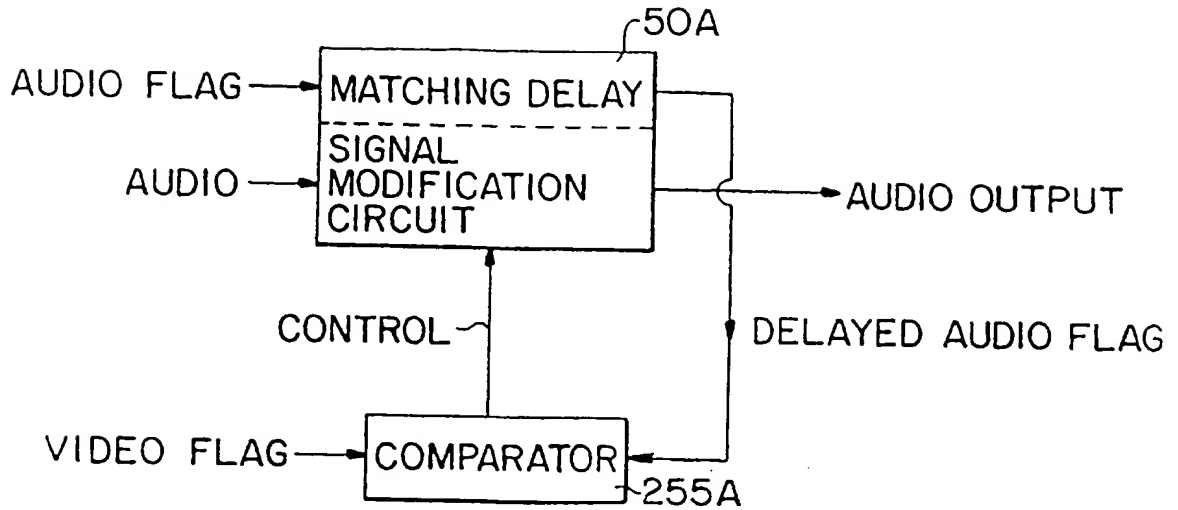


FIG. 30

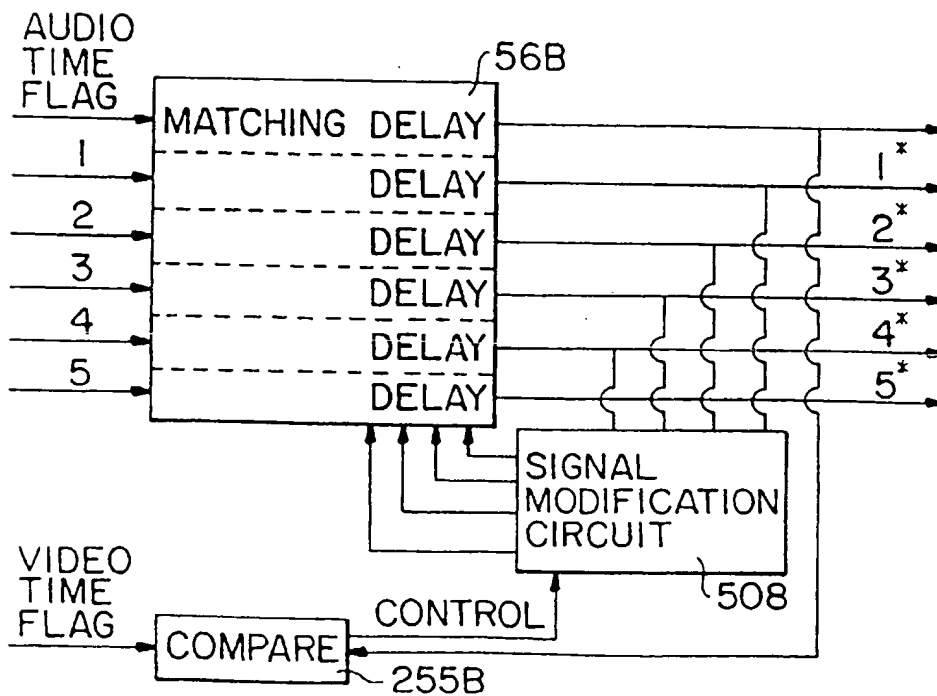
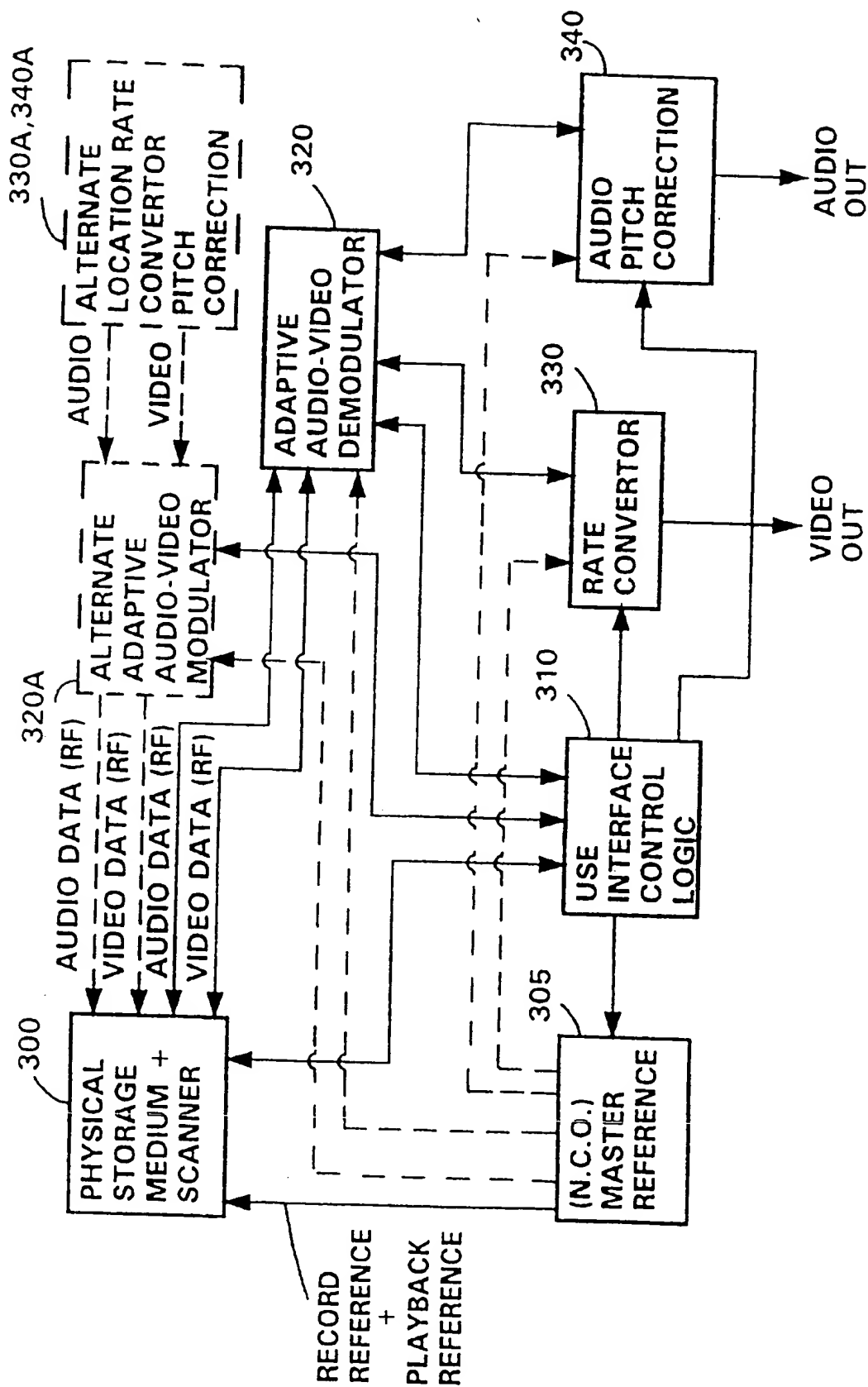


FIG. 31



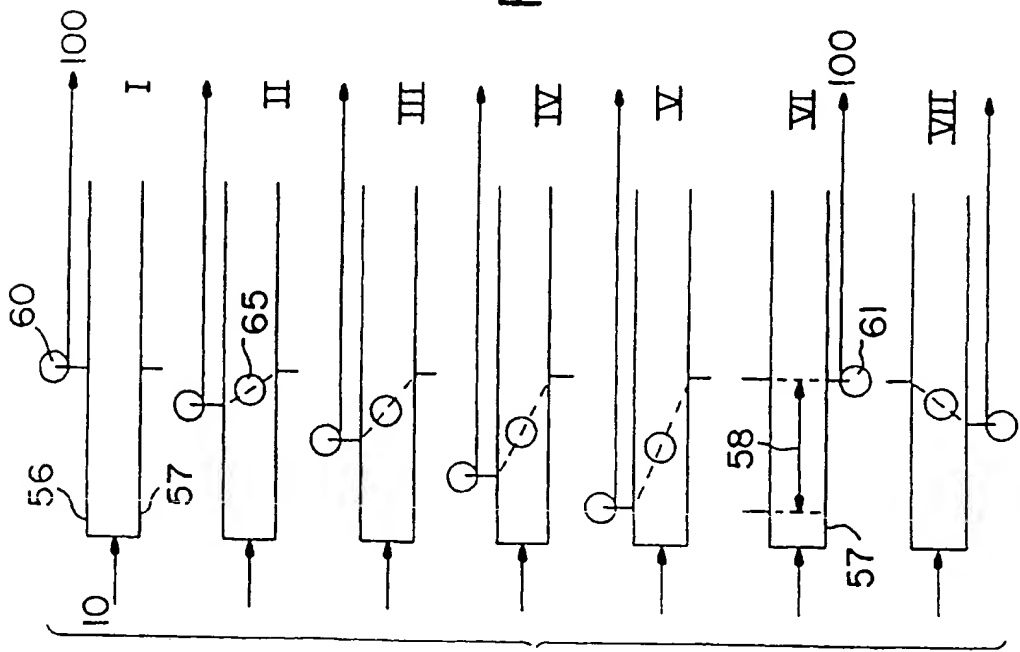


FIG. 32A

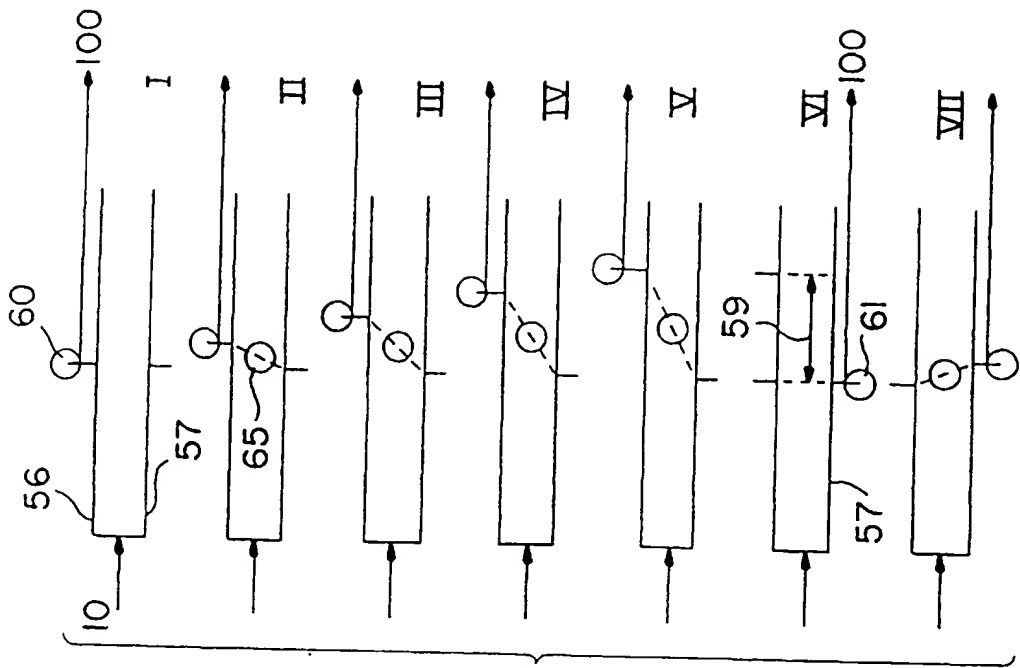


FIG. 32B

FIG. 33

